WHAT IS CLAIMED IS:

1. A programmable logic device comprising:

memories for logic which are arranged in series to store LUTs (look up tables) of logic functions;

plural external input lines for input variables connecting to said memories for logic;

one or more memories for interconnection which store(s) information for connection how to select either output lines of said memory for logic of the preceding stage or said external input lines connecting to each input line of said memory for logic of the succeeding stage; and

one or more reconfigurable interconnection circuits which connect(s) the output lines of said memory for logic of the preceding stage or the external input lines with the input lines of said memory for logic of the succeeding stage according to the output of said memory for interconnection.

2. A programmable logic device comprising:

memories for logic arranged in a circular shape to store LUTs of logic functions;

plural external input lines for input variables connecting to said memories for logic;

one or more memories for interconnection which store(s) information for connection how to select either output lines of said memory for logic of the preceding stage or said external input lines connecting to each input line of said memory for logic of the succeeding stage; and

one or more reconfigurable interconnection circuits which connect(s)

the output lines of said memory for logic of the preceding stage or the external input lines with the input lines of said memory for logic of the succeeding stage according to the output of said memory for interconnection.

3. The programmable logic device according to claim 1 or 2:

comprising external output lines which send out the result of logic operation to the external circuit; and wherein

said memory for interconnection stores information for connection how to select output lines of said memory for logic of the preceding stage that connect to said external output lines;

said interconnection circuit connects the output lines of said memory for logic of the preceding stage with said external output lines according to the output of said memory for interconnection.

4. The programmable logic device according to any of claims 1 to 3:

comprising means to store the designator for block which stores the variable for designating block to specify the block in the memory for logic; and wherein

said interconnection circuit connects the output lines of said memory for logic of the preceding stage, the external input lines, and the output lines of means to store the designator for block with the input lines of said memory for logic of the succeeding stage, according to the output of said means to store the designator for block,

so that input variables from outputs of said memory for logic of the preceding stage and said external input lines, are sent to the memory area of said memory for logic of the succeeding stage which is specified by

variable for designating block,

or so that input variables from output of the memory block of said memory for logic of the preceding stage which is specified by variable for designating block and said external input lines, are sent to said memory for logic of the succeeding stage.

5. The programmable logic device according to any of claims 1 to 4 comprising:

an intermediate variable register which stores outputs of said memories for logic and sends them to the inputs to succeeding said memory for logic activated by the external data strobe signal.

6. The programmable logic device according to any of claims 1 to 5 comprising:

bypass lines to connect inputs with outputs of said intermediate variable register; and

bypass selection circuits that select either the output lines of said intermediate variable register or said bypass lines, and produce the signal of the selected lines.

7. The programmable logic device according to claim 5 or 6 comprising: means to designate the memory for logic which specifies the index of said memory for logic to perform the operation by counting the number of said data strobe signals.

8. The programmable logic device according to any of claims 5 to 7

comprising: means for power control that set said memories for logic performing the operations to the normal mode and other memories for logic to the low power mode.

9. The programmable logic device according to any of claims 1 to 8: wherein the input lines of part of said memory for logic are directly connected to said external input lines without passing through said interconnection circuit.

10. The programmable logic device according to any of claims 1 to 9: wherein the output lines of part of said memory for logic are directly connected to the input line of part of the memory for logic in the succeeding stage, without passing through said interconnection circuit.

11. The programmable logic device according to any of claims 1 to 10: wherein

said interconnection circuit comprises selectors; and

each said selector selects

either an output line of said memory for logic in the preceding stage or an external input line, or

either an output line of said memory for logic in the preceding stage, said external input line, or an output line of the mean to store the designator for block, and

connects to the input line of memory for logic in the succeeding stage, according to the output values of said memory for interconnection.

12. The programmable logic device according to any of claims 1 to 11: wherein

said interconnection circuit comprises a shifter where output lines of said memory for logic in the preceding stage are shifted to connect to the input line of said memory for logic in the succeeding stage, according to the output values of said memory for interconnection.

13. The programmable logic device according to any of claims 1 to 12: wherein

said interconnection circuit comprises multiplexers; and

said each multiplexer selects one line out of the plural output lines of said memory for logic in the preceding stage and the plural external input lines, and connects it to an input line of said memory for logic in the succeeding stage, according to the output values of said memory for interconnection.